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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,755	04/21/2004	Charles A. Miller	FACT-01005US0	5339

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EXAMINER	
NGUYEN, JIMMY	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/828,755	MILLER ET AL.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 - 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 –5, 7, 15, 18, 19, 28, 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu et al (US 6,400,173).

As to claim 1, Shimizu et al disclose (fig 1) a probe card assembly comprising a programmable controller (5) to control the provision of test signals to test probes (6) of the probe card (2) for testing components on a wafer (W).

As to claim 2, Shimizu et al disclose (fig 1) A probe card assembly of claim 1, wherein the programmable controller (5) comprises a Field Programmable Gate Array (FPGA) (column 6line 23 – 25).

As to claim 3, Shimizu et al disclose (fig 1) the probe card assembly of claim 1, wherein the programmable controller (5) is connected through an interface (by the cable and substrate 4) to a test system controller (3), where the test system controller (3) provides test
signals (Writing DATA) to the interface to control testing of components on a wafer (W).

As to claim 4, Shimizu et al disclose (fig 1) the probe card assembly of claim 3, wherein the interface comprises one or more of a group consisting of a serial (each FPGA 5 directly connected to chip under test).

As to claim 5, Shimizu et al disclose (fig 1) the probe card assembly of claim 1, further comprising a memory (within the controller 3) accessible by the programmable controller (5), wherein the memory stores a test program enabling the programmable controller to perform testing of components on the wafer (W).

As to claim 7, Shimizu et al disclose (fig 9a) the probe card assembly of claim 1, wherein programmable controller (5) is configured to perform self testing of components included in the probe card assembly.

As to claim 15, Shimizu et al disclose (fig 9a) a probe card assembly of claim 1 further comprising: a space transformer (4) supporting the test probes (6) and having internal routing lines connected to the test probes (6), wherein the space transformer (4) supports the programmable controller (5).

As to claims 18, 19, Shimizu et al disclose (fig 1) the test program loaded into the FPGA (5) is provided from a CAD design system used to develop the components on the wafer (W).

As to claim 28, Shimizu et al disclose (fig 1 and 9a) a probe card assembly comprising a programmable controller (3) configured to perform self testing (tester build in chip) of components included in the probe card assembly.

As to claim 29, Shimizu et al disclose (fig 1 and 9a) a probe card assembly comprising a serial interface device (4) configured to connect to a test system controller (3) to receive test signals for distributing to probes (6) of the probe card assembly (2).

4. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Miller (US 6,798,225).

As to claim 17, Miller disclose a probe card assembly comprising:

Isolation buffers, each of the isolation buffers (Rn) connected in series between a single tester channel (57) and a plurality of test probes thus providing isolation of the test probes.

5. Claims 20 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Sporck et al (US 6,856,150).

As to claim 20, Sporck et al disclose (fig 4) a probe card assembly comprising: a daughter card (432) connected to a base PCB (402), the base PCB (402) including connectors (430) for connecting to a test system controller (not shown) and routing lines from the connectors to contacts providing electrical connections to test probes (408) for contacting DUTS of a wafer, the daughter card including discrete components (702, fig 7) configured for providing additional signals to the DUTS.

As to claim 21, Sporck et al disclose (fig 4) the daughter card (432) is connected to the PCB (402) by removable connectors (434, 414).

As to claims 22, 23, Sporck et al disclose (fig 4) the probe card assembly of claim 10, wherein the components (CH, chip) on the wafer (W) include microprocessors, and wherein the discrete components comprise support circuits for a personal computer motherboard.

6. Claims 24, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Leas et al (US 6,351,134).

As to claim 24, Leas et al disclose (figs 1 and 2) a probe card assembly comprising:

power supply isolation devices (40) connected in series with multiple power supply lines that distribute power from a single power supply line (PS) of a test system controller to multiple test probes, each test probe configured to contact a DUT power supply input, wherein the power supply isolation devices (40) are configured to minimize current flow on a given one of the power supply lines when a DUT (37) on the given line is determined to be faulty.

As to claim 25, Leas et al disclose (figs 1 and 2) the probe card assembly of claim 24, wherein the power supply isolation devices comprise one or more of a group consisting of voltage regulators (40, each DUT 37 has its own voltage regulators 40).

7. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Nelso et al (US 5,550,480).

As to claim 27, Nelson et al disclose (fig 4) a probe card assembly comprising: a DC-DC converter (Vref3, column 7 lines 11 – 16) connected (when the multiple probes contact with the wafer 16) between the single power supply line Vref4) of a test system controller (51), the power supply line (Vref4) distributing power through line branches to multiple test probes 25, 20), the DC-DC converter (Vref 3) configured to increase current in a signal provided on the power supply line.

7. Claims 33 – 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Lino et al (US 6,380,753).

As to claim 33, Lino et al teach (fig 2) a probe card assembly comprising: a serial digital to analog converter (26) configured to serially receive digital test signal that are to be distributed to test probes of the probe card (13) in analog form the digital to analog converter (25) configured to convert and provide the test signal to the test probes in analog form.

As to claim 34, Lino et al teach (fig 2) an ADC configured to receive an analog signal from a test device and to send a digital representation to a test system controller

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6, 8, 9, 30, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al (US 6,400,173) in view of Lino et al (US 6, 380,753).

As to claims 6, 8, 30, 31, Shimizu et al disclose (fig 1) disclose everything except for the programmable controller comprises a serial to parallel converter configured to receive the test signals, the programmable controller configured to convert the test serial from serial to parallel and distribute the test signals in parallel to the test probes.

On the other hand, Lino et al teach (fig 2) the programmable controller (13) comprises a serial to parallel converter (31) configured to receive the test signals (from 12), the programmable controller (13) configured to convert the test serial from serial to parallel (fan out the test signal) and distribute the test signals in parallel to the test probes and the serial to parallel converter comprises a FPGA .

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al with the multiplexer of Lino et al for the purpose of fanning out the test signal.

As to claim 9, Shimizu et al disclose (fig 1) disclose everything except for a serial digital to analog converter connected to receive digital test signals from the programmable controller, the digital to analog converter configured to convert and provide the test signals to the test probes in analog form.

On the other hand, Lino et al teach (fig 2) a serial digital to analog converter (25) connected to receive digital test signals from the programmable controller, the digital to analog converter configured to convert and provide the test signals to the test probes in analog form.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al with the DAC of Lino et al for the purpose of converting signal from one form to another.

10. Claims 10, 11, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al (US 6,400,173) in view of Sporck et al (US 6, 856,150).

As to claim 10, Shimizu et al disclose (fig 1) disclose everything except for a daughter card connected to a base PCB, the base PCB including the programmable controller and connectors for connecting to a test system controller and routing lines from the connectors to contacts providing electrical connections to the test probes for

contacting DUTS on a wafer, the daughter card supporting discrete components configured for providing additional signals to the DUTS.

On the other hand, Sporck et al teach (fig 4) a daughter card (432) connected to a base PCB (402), the base PCB (402) including the programmable controller (702, fig 7 and column 4 lines 63 – 65) and connectors for connecting to a test system controller (tester, not shown) and routing lines from the connectors to contacts providing electrical connections to the test probes (408) for contacting DUTS on a wafer, the daughter card (432) supporting discrete components (702,fig 7, column 4 lines 61 – 63) configured for providing additional signals to the DUTS.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al with the daughter card of Sporck et al for the purpose of providing additional space on the probe card to allow for the use of larger probe head assemblies while not interfering with connections between the semiconductor tester and the probe card (column 3 lines 15 – 23).

As to claim 11, Sporck et al disclose the discrete components (702, fig 7 and column 4 lines 63 – 65) comprise an additional programmable controller.

As to claim 13, Shimizu et al disclose (fig 1) the probe card assembly of claim 10, wherein the components (CH, chip) on the wafer (W) include microprocessors, and

wherein the discrete components comprise support circuits for a personal computer motherboard.

As to claim 14, Shimizu et al disclose (fig 1) disclose everything except a daughter card connected to a base PCB, the base PCB including connectors for connecting to a test system controller and routing lines from the connectors to contacts providing electrical connections to the test probes for contacting DUTS on a wafer, the daughter card supporting the programmable controller.

On the other hand, Sporck et al teach (fig 4) a daughter card (432) connected to a base PCB (402), the base PCB (402) including connectors (430) for connecting to a test system controller (tester, not shown, column 4 lines 43 – 45) and routing lines from the connectors to contacts providing electrical connections to the test probes (408) for contacting DUTS on a wafer, the daughter card (432) supporting the programmable controller (702, fig 7).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al with the daughter card of Sporck et al for the purpose of providing additional space on the probe card to allow for the use of larger probe head assemblies while not interfering with connections between the semiconductor tester and the probe card (column 3 lines 15 – 23).

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al (US 6,400,173) in view of Sporck et al (US 6, 856,150) and further in view of Nelso et al (US 5,550,480).

As to claim 12, Shimizu et al and Sporck et al disclose disclose everything except for a DC-DC converter connected between the single power supply line of a test system controller, the power supply line distributing power through line branches to multiple test probes, the DC-DC converter configured to increase current in a signal provided on the power supply line.

On the other hand Nelson et al disclose (fig 4) a probe card assembly comprising:

a DC-DC converter (Vref3, column 7 lines 11 – 16) connected (when the multiple probes contact with the wafer 16) between the single power supply line Vref4) of a test system controller (51), the power supply line (Vref4) distributing power through line branches to multiple test probes 25, 20), the DC-DC converter (Vref 3) configured to increase current in a signal provided on the power supply line.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al and Sporck et al with DC/DC converter as taught by Nelso for the purpose of increasing the current to DUT.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al (US 6,400,173) in view of Miller (US 6,798,225).

As to claim 16, Shimizu et al disclose (fig 1) disclose everything except for resistors, each of the resistors connected in series between a single test system controller channel and a plurality of test probes thus providing resistive isolation of the test probes.

On the other hand, Miller teach (fig 5) the resistors (Rn) , each of the resistors (Rn) connected in series between a single test system controller channel(57) and a plurality of test probes thus providing resistive isolation of the test probes.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to use the resistor connected with the tester channel for the purpose of eliminating the signal reflection.

13. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leas et al (US 6,351,134) and further in view of Sporck et al (US 6, 856,150).

As to claim 26, Leas et al disclose (figs 1 and 2) a probe card assembly comprising:

power supply isolation devices (40) connected in series with multiple power supply lines that distribute power from a single power supply line (PS) of a test system controller to multiple test probes, each test probe configured to contact a DUT power supply input, wherein the power supply isolation devices (40) are configured to minimize current flow on a given one of the power supply lines when a DUT (37) on the given line is determined to be faulty and a space transformer (16) supporting the test probes (31) the

power supply isolation devices (40) are provided on at least one of the space transformer (16).

However, Leas et al are silent on

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one daughter card, wherein the power supply isolation devices are provided on at least one of the space transformer, the base PCB, and the at least one daughter card.

On the other hand, Sporck et al teach (fig 4A)

at least one daughter card (432); and

a base PCB (402) electrically interconnected with the space transformer (406) and the at least one daughter card (432),

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Leas et al with the daughter card of Sporck et al for the purpose of providing additional space on the probe card to allow for the use of larger probe head assemblies while not interfering with connections between the semiconductor tester and the probe card (column 3 lines 15 – 23).

14. Claims 32, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al (US 6,400,173) in view of Lino et al (U, 6,380,753).

As to claims 32, 35, Shimizu et al disclose (fig 1 and 9a) a probe card assembly comprising a serial interface device (4) configured to connect to a test system controller (3) to receive test signals for distributing to probes (6) of the probe card assembly (2) and a space transformer (4) to support the test probe (6).

However, Shimizu et al are silent on

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one daughter card, wherein serial to parallel converter, ADC, DCA are provided on at least one of the space transformer, the base PCB, and the at least one daughter card.

On the other hand, Lino et al teach (fig 2)

at least one daughter card (13); and

a base PCB (15) electrically interconnected with the space transformer (17) and the at least one daughter card (13), wherein serial to parallel converter (31) , ADC (26), DCA (25) are provided on at least one daughter card (13)

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test system of Shimizu et al with the daughter card of Lino et al for the purpose of providing additional space on the probe card to allow for the use of larger probe head assemblies while not interfering with connections between the semiconductor tester and the probe card.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is (703) 306-5858. The examiner can normally be reached on M- Ffrom 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramitez Nestor, can be reached on 571 – 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/19/05

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